1. A communication system for providing high speed communications between first and second locations, said communication system comprising:

a first clock resident or derived at said first location, said first clock related to a transmission rate;

a second clock related to a network link rate;

a phase device operable to generate a phase error signal as a function of said transmission rate and said network link rate;

a network coupling a transmitter at said first location to a receiver present at said second location;

wherein said transmitter is operable to transmit to said receiver both a data stream synchronized with said network link rate and said phase error signal; and

wherein said receiver is operable to recover an estimate of said transmission rate as a function of said phase error signal and said network link rate.

2. A communication system as recited in claim 1, wherein said first clock and said second clock have a predefined relation, and said phase device is operable to generate signals from said first and said second clocks, said signals having a nominal frequency rate rendering phase comparison of said first and said second clocks possible.

3. A communication system as recited in claim 2, wherein said phase device is a component of said transmitter .

4. A communication system, wherein said transmitter is operable to transmit said phase error signal in an overhead channel.

5. A transmitter circuit for use in a data communications system, said transmitter circuit operable to transmit data at a synchronized rate, said transmitter circuit comprising:

a first variable modulus counter having a first clock input, a first control input, and a first output, said first clock input intended for coupling to a transmitter clock, said first variable modulus counter controllable to divide the frequency of the transmitter clock by a first integer adjustable by an arbitrary integer offset +/- N;

a second variable modulus counter having a second clock input, a second control input, and a second output, said second clock input intended for coupling to a network link clock, the frequency of said network link clock having a predetermined relationship to the frequency of the transmitter clock, said second variable modulus counter controllable to divide the frequency of the network link clock by a second integer adjustable by an arbitrary integer offset +/- M;

wherein said first and second integers are selected such that outputs of said first and said second variable modulus counters have an identical nominal frequency;

a detector having a first input coupled to said first output, a second input coupled to said second output, and a detector output, said detector operable to generate a phase error signal reflective of a phase difference between said signals generated at said first and second outputs; and

a modulus control circuit responsive to said phase error signal to control said first and second variable modulus counters.

6. A transmitter circuit as recited in claim 5, wherein said integer N is the number "1," and said integer M is the number "1."

7. A transmitter circuit as recited in claim 5, wherein said detector generates said phase error signal as a quantized bit of information.

8. A transmitter circuit as recited in claim 7, wherein said transmitter circuit is further operable to transmit data at a rate synchronized with said network link clock.

9. A transmitter circuit as recited in claim 8, wherein said network link clock is further operable to transmit said quantized bit in an overhead channel.

10. A transmitter circuit as recited in claim 9, wherein said quantized bit is transmitted at a frequency rate substantially lower than the frequency rate of said transmitter clock.

11. A transmitter circuit as recited in claim 10, wherein the frequency of said transmitter clock is about 44.736 MHz, the frequency of said network link clock is about 35.328 MHz, said nominal rate is about 8 kHz, and the frequency rate of transmission of said quantized bit is about or less than 8 kHz.

12. A transmitter circuit as recited in claim 5, wherein said transmitter circuit is one component of a high speed modem.

13. A receiver circuit for use in a data communications system, said receiver circuit operable to receive data and to recover transmit timing data and synchronize received data according to recovered transmit timing data, said receiver circuit comprising:

a first variable modulus counter controllable to frequency divide a first input signal by a first integer adjustable by an arbitrary integer offset +/- N to generate a first output signal;

a second variable modulus counter controllable to frequency divide a second input signal by a second integer adjustable by an arbitrary integer offset +/- M to generate a second output signal;

a detector circuit operable to determine a phase relation between said first and second output signals;

an oscillator circuit controlled by said phase relation, said oscillator providing feedback to said second variable modulus controller;

a modulus control circuit responsive to received timing data, said modulus control circuit operable to control said first and second variable modulus counters,

whereby said receiver circuitry reaches a steady state and generates a clock signal for synchronizing received data around recovered phase variation information.

14. A receiver circuit as recited in claim 13 further comprising:

circuitry for receiving primary transmitted data; and

circuitry for recovering received timing data from within an overhead channel.

15. A receiver circuit as recited in claim 13 further comprising:

a lowpass filter coupled between said phase detector circuit and said oscillator circuit.

16. A method for timing generation and recovery in a communications system requiring synchronization, the method comprising:

providing a master clock signal and a network link clock signal at a transmitter;

calculating a phase relation between said master clock signal and said network link clock signal;

via said transmitter, transmitting data to a receiver at first rate specified by said network link clock signal; and

via said transmitter, transmitting said phase relation to said receiver.

17. A method as recited in claim 16, the method further comprising:

via said receiver, receiving said data and said phase relation;

providing said network link clock signal at said receiver; and

via said receiver, recovering an estimate of said master clock signal.

18. A method for timing generation and recovery in a communications system as recited in claim 16, wherein:

calculating said phase relation includes quantizing said phase relation; and

said quantized phase relation is transmitted via an overhead channel.

19. A method as recited in claim 16, wherein said master clock signal and said network link clock signal have a fixed relation defined by a first integer and a second integer, wherein calculating said phase relation includes:

frequency dividing said master clock signal by (said first integer plus a phase correction +/- N) in order to generate a first signal of substantially a nominal rate;

frequency dividing said network link clock signal by (said second integer plus a phase correction +/- M) in order to generate a second signal of substantially a nominal rate;

determining said phase relation by comparison of said first signal with said second signal; and

determining said phase corrections +/- N and +/- M in an ongoing fashion.

20. A method as recited in claim 19, wherein said phase relation is quantized.

21. A method as recited in claim 19, wherein said phase relation is transmitted via an overhead channel at a frequency equal to or lower than said nominal rate.